WHAT IS CLAIMED:

1. A semiconductor device comprising:

a semiconductor region of a first conductivity type;

a source region of a second conductivity type in one side of the semiconductor region;

a drain region of the second conductivity type in the one side of the semiconductor region and spaced apart from the source region;

trenches in the one side of the semiconductor region, between the source region and the drain region, and spaced apart laterally from the source region;

an insulator filling each of the trenches;

a drain drift region of the second conductivity type in the semiconductor region, the drain drift region being connected to the drain region, the drain drift region extending along side and bottom walls of the trenches, the drain drift region being spaced apart from the source region;

a gate insulation film on the surface of the semiconductor region between the source region and the drain drift region;

a gate electrode on the gate insulation film;

a source electrode connected electrically to the source region;

a drain electrode connected electrically to the drain region; and

a first triple layer structure formed of the drain drift region, the semiconductor region, and the drain drift region, the triple layer structure being between the adjacent trenches such that the drain drift region is between the adjacent trenches,

wherein the trenches are aligned in the width direction of the channels formed beneath the gate insulation film.

2. The semiconductor device according to claim 1, further including a well region of the first conductivity type doped more heavily than the semiconductor region, the drain drift region being in the well region, and a second triple layer structure formed of the drain drift region, the well region, and the drain drift region formed between the adjacent trenches.

3. The semiconductor device according to claim 1, further including one or more electric field relaxation layers of the first conductivity type in the drain drift region, and along the trenches.

4. The semiconductor device according to claim 2, further including one or more electric field relaxation layers of the first conductivity type in the drain drift region, and along the trenches.

5. The semiconductor device according to claim 3, wherein the one or more electric field relaxation layers are in the drain drift region between adjacent trenches.

6. The semiconductor device according to claim 4, wherein the one or more electric field relaxation layers are in the drain drift region between adjacent trenches.

7. The semiconductor device according to claim 1, further including one or more electrical conductors in the insulator in each of the trenches, and extending parallel to a side wall of the trenches formed between adjacent trenches.

8. The semiconductor device according to claim 2, further including one or more electrical conductors in the insulator in each of the trenches, and extending parallel to a side wall of the trenches formed between adjacent trenches.

9. The semiconductor device according to claim 3, further including one or more electrical conductors in the insulator in each of the trenches, and extending parallel to a side wall of the trenches formed between adjacent trenches.

10. The semiconductor device according to claim 4, further including one or more electrical conductors in the insulator in each of the trenches, and extending parallel to a side wall of the trenches formed between adjacent trenches.

11. The semiconductor device according to claim 5, further including one or more electrical conductors in the insulator in each of the trenches, and extending parallel to a side wall of the trenches formed between adjacent trenches.

12. The semiconductor device according to claim 6, further including one or more electrical conductors in the insulator in each of the trenches, and extending parallel to a side wall of the trenches formed between adjacent trenches.

13. The semiconductor device according to 3, wherein each of the one or more electric field relaxation layers is on the boundary between the drain drift region and the insulator in the trench.

14. The semiconductor device according to 4, wherein each of the one or more electric field relaxation layers is on the boundary between the drain drift region and the insulator in the trench.

15. The semiconductor device according to 5, wherein each of the one or more electric field relaxation layers is on the boundary between the drain drift region and the insulator in the trench.

16. The semiconductor device according to 6, wherein each of the one or more electric field relaxation layers is on the boundary between the drain drift region and the insulator in the trench.

17. The semiconductor device according to 7, wherein each of the one or more electric field relaxation layers is on the boundary between the drain drift region and the insulator in the trench.

18. The semiconductor device according to 8, wherein each of the one or more electric field relaxation layers is on the boundary between the drain drift region and the insulator in the trench.

19. A semiconductor device comprising:

a semiconductor region of a first conductivity type;

a source region of a second conductivity type in one side of the semiconductor region;

a drain region of the second conductivity type in the one side of the semiconductor region and spaced apart laterally from the source region;

trenches in the one side of the semiconductor region, between the source region and the drain region, and spaced apart from the source region;

an insulator filling each of the trenches;

a drain drift region of the second conductivity type in the semiconductor region, the drain drift region being connected to the drain region, the drain drift region extending along side and bottom walls of the trenches, the drain drift region being spaced apart from the source region;

a gate insulation film on the surface of the semiconductor region between the source region and the drain drift region;

a gate electrode on the gate insulation film;

a source electrode connected electrically to the source region;

a drain electrode connected electrically to the drain region; and

one or more electrical conductors in the insulator in each of the trenches, the one or more electrical conductors extending parallel to a side wall of the trench formed between adjacent trenches,

wherein the trenches are aligned in the width direction of the channels formed beneath the gate insulation film.

20. The semiconductor device according to claim 19, wherein the thickness of the insulator between the one or more electrical conductors and the side wall of the trench on the drain side is larger than the thickness of the insulator between the one or more electrical conductors and the side wall of the trench on the source side.